a' cont.

patterning said photoresist layer to provide a plurality of openings, said openings being spaced apart and exposing said insulating layer;

forming a barrier layer at a bottom of said openings in said photoresist layer over any exposed portions of said insulating layer;

partially filling said openings with a conductive material to form a conductive layer;

forming a silicon insulating layer over said conductive layer to completely fill said openings;

removing remaining portions of said photoresist;

forming a passivation layer on exposed sidewalls of said conductive layer; and

forming a plurality of trenches in said silicon substrate and between said openings.

93. (New) The method of claim 92, wherein said insulating layer is an oxide layer.

94. (New) The method of claim 92, wherein said openings have a width of 250,000 Angstroms to about 350,000 Angstroms.

95. (New) The method of claim 92, wherein said barrier layer comprises a bonding material selected from the group consisting of tantalum, titanium, titanium-tungsten, titanium nitride and chromium.

96. (New) The method of claim 92, wherein said conductive layer comprises copper.

a' Cont.

97. (New) The method of claim 92, wherein said conductive layer is formed to a thickness of about 100,000 Angstroms to about 200,000 Angstroms.

98. (New) The method of claim 92, wherein said silicon oxide layer is deposited by thermal evaporation at or near room temperature.

99. (New) The method of claim 99, wherein said silicon oxide layer is formed to a thickness of about 5,000 Angstroms to about 10,000 Angstroms.

100. (New) The method of claim 92, wherein said passivation layer is formed to a thickness of about 50 Angstroms to about 100 Angstroms.

101. (New) The method of claim 92, wherein said passivation layer is a silicide layer.

102. (New) The method of claim 92, wherein said trenches have a depth of about 100,000 Angstroms to about 200,000 Angstroms and a width of about 150,000 Angstroms.

103. (New) The method of claim 92, wherein said trenches are formed by reactive ion etching using a deep trench etcher at an etch rate of about 2.2 μm/min.

104. (New) The method of claim 92, wherein said trenches are formed by an isotropic etching process

105. (New) The method of claim 92, wherein said trenches have a circular shape with a radius of about 50,000 Angstroms to about 100,000 Angstroms.

(√) 106. (New) A method of forming a coplanar waveguide comprising the acts of:

depositing an oxide layer over a silicon substrate;

forming a photoresist layer over said oxide layer;

a' cont.

patterning said photoresist layer to provide a plurality of openings, said openings being spaced apart by about 150,000 Angstroms to about 200,000 Angstroms and exposing said oxide layer;

depositing a barrier layer at a bottom of said openings over any exposed portions of said oxide layer, wherein said barrier layer comprises a bonding material selected from the group consisting of tantalum, titanium, titanium-tungsten, titantium nitride and chromium;

depositing a copper layer by thermal evaporation in said partially filled openings to partially fill said openings;

forming a silicon oxide layer over said partially filled openings to completely fill said openings;

removing remaining portions of said photoresist to form a signal copper line;

forming a passivation layer on exposed sidewalls of said signal copper line; and

etching said silicon substrate between said openings and to a depth of about 100,000 Angstroms to about 200,000 Angstroms to form a plurality of trenches.

107. (New) The method of claim 106, wherein said copper layer has a thickness of about 100,000 Angstroms to about 200,000 Angstroms.

108. (New) The method of claim 106, wherein said copper layer is exposed to silane to form a silicide layer on sidewalls of said copper layer.

109. (New) The method of claim 108, wherein said copper layer is exposed to silane at 300° C to form said silicide layer.

REPLACEMENT CLAIMS

a2 Sub B'

1. (Amended) A method of forming a coplanar waveguide comprising the acts of:

forming a signal conductor line over a substrate;

forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line, said ground conductor plane being spaced from said signal conductor line; and

subsequently forming a trench in said substrate in an area between said at least one ground conductor plane and said signal conductor line.

a3 Sub B'

19. (Amended) A method of forming a coplanar waveguide comprising the acts of:

forming a signal conductor line over a silicon substrate;

forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line, said ground conductor plane being spaced from said signal conductor line; and

subsequently forming at least one trench in said silicon substrate in an area between said at least one ground conductor plane and said signal conductor line, said at least one trench having a depth of about 100,000 Angstroms to about 200,000 Angstroms and a width of about 100,000 Angstroms to about 150,000 Angstroms.

a4 Sub B'

~~32.~~ (Amended) A method of forming a coplanar waveguide comprising the acts of:

forming a signal conductor line over a silicon substrate;

a4 cont. Sub B'

forming at least one longitudinal ground conductor plane over said substrate and on a side of said signal conductor line, said ground conductor plane being spaced from said signal conductor line; and

forming at least one trench in said silicon substrate by use of an isotropic etching process in an area between said at least one ground conductor plane and said signal conductor line, said at least one trench having a radius of about 50,000 Angstroms to about 100,000 Angstroms.

a5 Sub B'

~~41. (Amended)~~ The method of claim 40, wherein said copper layer is exposed to silane at 300° C to form said silicide layer.